

### **REMARKS**

On August 17, 2005, a personal interview was conducted with Examiner Gurley, and after this interview it was believed that the claims as amended in accordance with the response filed August 22, 2005, would be allowed over the references relied upon at that time. Accordingly, upon receipt of the Final rejection mailed November 18, 2005, which basically repeated the previous rejections, Applicant's undersigned representative spoke with Examiner Gurley via telephone on December 30, 2005, to inquire as to why these rejections were being maintained. After discussion of the claims and the relied upon references, Examiner Gurley stated that upon the filing of a response that basically repeats the arguments presented on August 22, 2005, the current rejections of record would be withdrawn.

Accordingly, the Remarks forming part of the response filed August 22, 2005, are hereby repeated, and the following additional remarks are provided.

Regarding Ohno, this reference discloses, as shown in Figs. 10B-15, a method for forming a semiconductor device which has sidewalls 21B, an etching-stop layer 40, and an insulating interlayer 41 on substrate 10. Each sidewall 21B is formed so as to cover a corresponding side face of each gate electrode 14B. In addition to sidewalls 21B, the semiconductor device of Ohno has two different dielectric films in the spaces between adjacent gate electrodes 14b; namely the etching-stop layer 40 and the insulating interlayer 41.

To the contrary, each of the independent claims recites a method for forming a semiconductor device including, in part, forming gate electrodes and forming a first dielectric film on a substrate. Thus, as shown in Figs. 1A-1E, for example, the semiconductor device of the instant invention includes, in addition to sidewalls 3, first dielectric film 4 between adjacent gate electrodes 2.


Accordingly, where there are two dielectric films in the semiconductor device manufactured in accordance with the method of Ohno, there is but a single dielectric film in the semiconductor device manufactured in accordance with the claimed method.

In view of the above, it is respectfully submitted that the application is in condition for allowance, with the allowed claims being 15-17, 22, 24, 26-33 and 35-65, and an early Notice of Allowance is earnestly solicited.

If after reviewing this Amendment, the Examiner believes that any issues remain which must be resolved before the application can be passed to issue, the Examiner is invited to contact the Applicant's undersigned representative by telephone to resolve such issues.

Respectfully submitted,

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February 21, 2006